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Eight In. Wafer-Scale Epitaxial Monolayer MoS_2

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Large-scale, high-quality, and uniform monolayer molybdenum disulfide (MoS_2) films are crucial for their applications in next-generation electronics and optoelectronics. Epitaxy is a mainstream technique for achieving high-quality MoS_2 films and is demonstrated at a wafer scale up to 4-in. In this study, the epitaxial growth of 8-in. wafer-scale highly oriented monolayer MoS_2 on sapphire is reported as with excellent spatial homogeneity, using a specially designed vertical chemical vapor deposition (VCVD) system. Field effect transistors (FETs) based on the as-grown 8-in. wafer-scale monolayer MoS_2 film are fabricated and exhibit high performances, with an average mobility and an on/off ratio of 53.5 cm^2 V^{-1} s^{-1} and 10^7, respectively. In addition, batch fabrication of logic devices and 11-stage ring oscillators are also demonstrated, showcasing excellent electrical functions. This work may pave the way of MoS_2 in practical industry-scale applications.

1. Introduction

2D semiconductors have attracted tremendous interests for next-generation electronic and optoelectronic applications owing to their unique physical and chemical properties.[1–14] To realize practical applications, it is crucial to start with high-quality 2D semiconductors films on an industrial-scale. Notably, 12-in. wafer-scale monolayer MoS_2 films have been recently demonstrated.[15–17] However, these large monolayer MoS_2 films are polycrystalline with dense misoriented grain boundaries (GBs), which degrade both their electrical transport properties through scattering charge carriers and mechanical properties by disrupting the structure and causing instability.[18–22] In order to reduce such detrimental GBs, epitaxial growth is considered an effective strategy.[23–25] Unfortunately, the epitaxy of 2D semiconductors is limited to a maximum wafer size of 4 in.

Aiming to further scale up the epitaxial 2D semiconductor wafers, we report, in this work, the epitaxial growth of monolayer MoS_2 at a record-high 8-in. wafer scale on single-crystal sapphire substrates using a home-made VCVD approach. The epitaxial MoS_2 monolayers are uniform across the entire 8-in. wafer and consist of only two anti-parallel domain orientations with largely suppressed misoriented GBs. These 8-in. wafer-scale monolayers also exhibit reasonably high electrical quality with an average electron mobility of 53.3 cm^2 V^{-1} s^{-1} (highest at 75.2 cm^2 V^{-1} s^{-1}) and on/off ratio of more than 10^7 for FETs. Besides, we also demonstrate the batch fabrication of logic devices and ring oscillators using these 8 in. of monolayer MoS_2 wafers.

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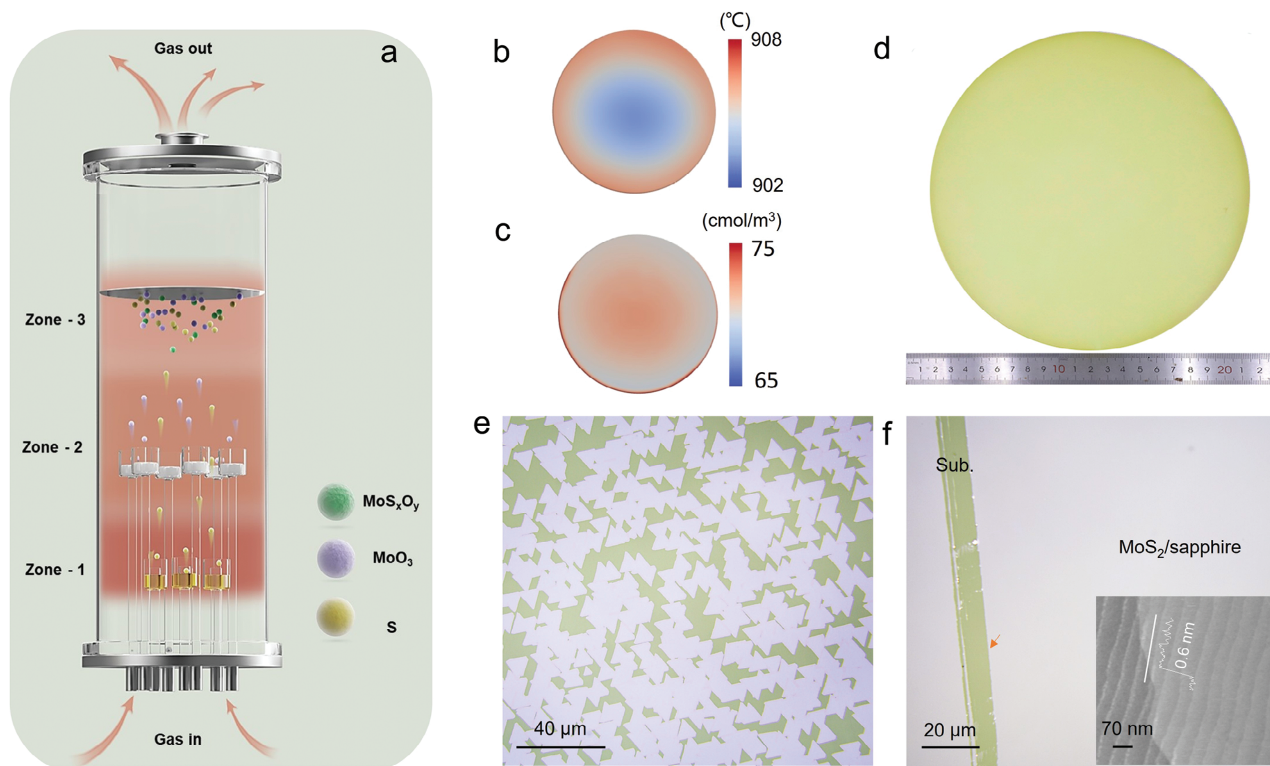

Figure 1. Epitaxy of 8-in. monolayer MoS_2 on sapphire wafers. a) Schematic of VCVD setup. S (MoO_3) sources are loaded in three (six) independent containers flowing with carrier gases and located at the temperature zone-1 (zone-2), and the substrate is loaded at the temperature zone-3. b) The simulated temperature distribution on the substrate surface at a temperature of 930 °C for zone-3. c) The simulated carrier gas concentration distribution on the substrate surface. d) Photograph of a typical as-grown 8-in. monolayer MoS_2 wafer. e) Optical microscope image of the synthesized MoS_2 after 30 min of growth. Orientated domains can be seen in an antiparallel manner. f) Optical microscope image of monolayer MoS_2 on sapphire. Inset shows the AFM image of the red arrow area.

2. Epitaxy of MoS_2 on Sapphire by VCVD

To achieve large-area, high-quality epitaxial growth, we use 8-in. single-crystal sapphire wafers as substrates. Note that sapphire substrates have been widely used in the previous growth of monolayer transition-metal dichalcogenides (TMDCs) films.[25–28] In general, a wafer-scale epitaxy of monolayer TMDCs starts from discrete nucleation and enlargement into domains to further domain growth, and finally, stitch into a continuous film. Regardless of the different reaction sources used, it is requisite to have uniform source flux reaching to the substrate surface during the growth to guarantee a uniform growth of monolayer TMDCs at wafer scale. With this concern, we thus designed a VCVD system for 8-in. wafer-scale monolayer MoS_2 growth, as shown in **Figure** 1a; Data S1, Supporting Information. In this system, the substrate (placed in the top chamber) was designed to face the multiple reaction sources (placed in the bottom chamber) directly to realize a uniform source flux evaporated onto the substrate surface. The anti-gravity direction transport of reaction sources could also effectively avoid the agglomerates of condensed and particulate sources from reaching the substrate surface to cause localized uncontrollable growth.[29,30] In addition, three sulfur sources and six MoO_3 sources were placed independently and with spatial symmetry to provide uniform evaporation flux. The flux of these sources could be well controlled by adjusting the evaporation temperature and flow rate of the carrier gas. According to our computational fluid dynamics simulations, the distribution of temperature and carrier gas concentration across the 8-in. substrate surface varied by 0.26% and 4.5%, as shown in Figure 1b,c, respectively. Such small variations guaranteed the uniform growth of monolayer MoS_2 at 8-in. wafer scale.

Figure 1d shows an as-grown 8-in. monolayer MoS_2 wafer. Typically, the as-grown MoS_2 film consists of domains (at an average size around tens of micrometers) aligned in two antiparallel orientations which are energetically equal on sapphire (0001) surfaces (Figure 1e; Figure S2a,b, Supporting Information). Figure 1f shows the optical microscope image of full-coverage monolayer MoS_2 on sapphire surface with a scratch to guide viewing. Please refer to Video S1, Supporting Information, for further confirmation at the 8-in. wafer scale. In addition, the surface morphology and thickness of the film were characterized by atomic force microscopy (AFM), as shown in the inset of Figure 1f. AFM results confirm the monolayer thickness of ≈0.6 nm.

3. Structural and Spectroscopic Characterizations

Figure 2a presents the X-ray photoelectron spectroscopy (XPS) of MoS_2 on sapphire, revealing characteristic peaks of S $2p_{3/2}$, $2p_{1/2}$, Mo $3d_{5/2}$, and Mo $3d_{3/2}$. The XPS analysis indicates the

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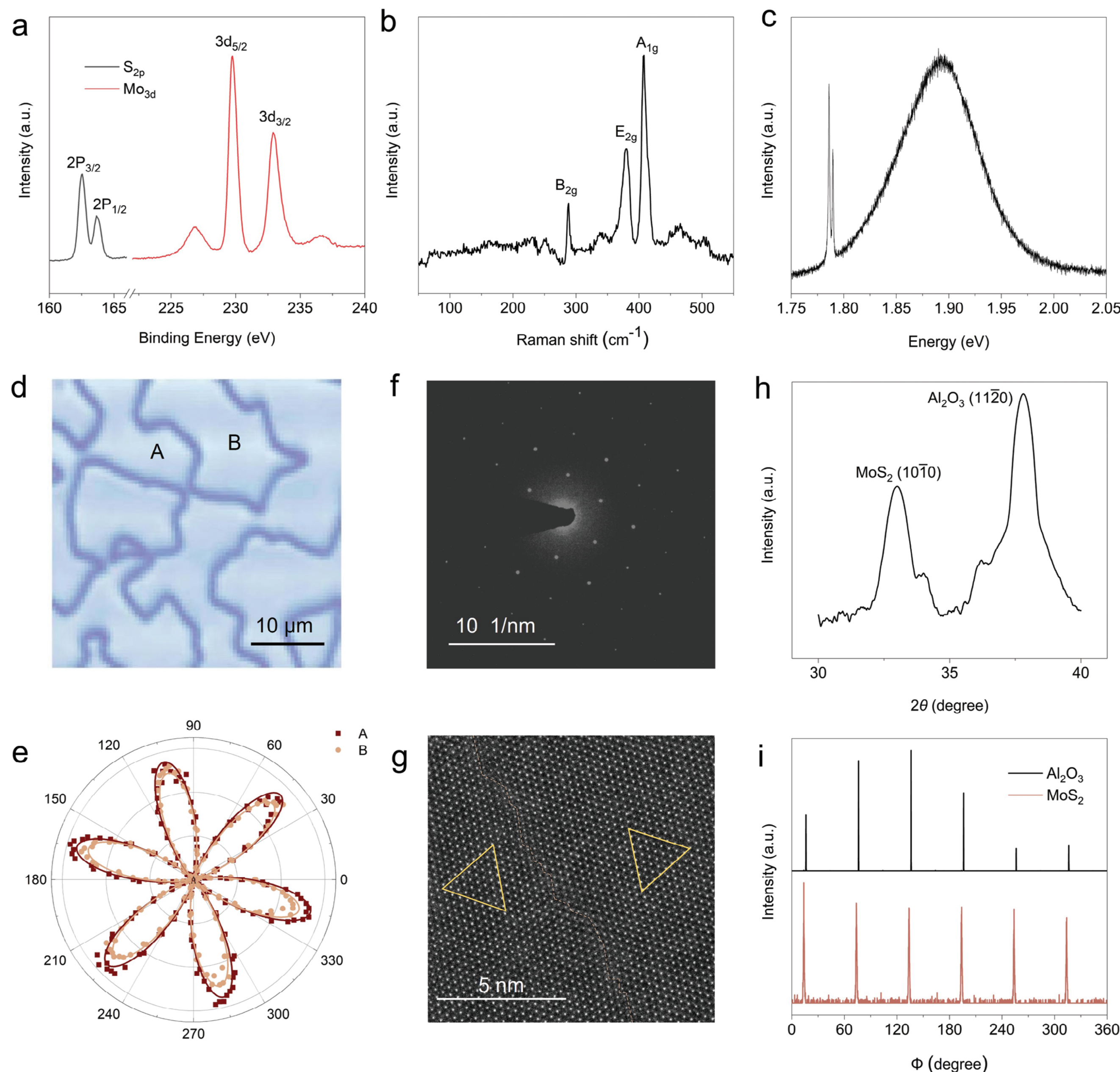

Figure 2. Highly oriented monolayer MoS_2 film. a–c) XPS, Raman, PL spectra of the as-grown O-doped monolayer MoS_2 film. d) SHG mapping of the highly oriented monolayer MoS_2 film with GBs clearly seen. e) Polar plots of the SHG intensity of the two grains (shown in [d]) on both sides of the GB. f) SAED pattern of the film with a selected area diameter of ≈1 µm. g) HRTEM image at the GB. Yellow triangles mark the orientation of domains and the dashed line marks the GB location. h) In-plane XRD θ–2θ diffractogram. i) In-plane φ-scan of $(10\bar{1}0)$ and $(11\bar{2}0)$ planes of the 8-in. MoS_2 and sapphire wafers, respectively.

presence of oxygen doping in the sample, and the doping level can be tuned by the flowed oxygen concentration (Figure S4a–c, Supporting Information). The substitutional doping of oxygen is confirmed from the Raman vibration peak of the Mo—O bond (B_{2g}) at 287 cm^{-1} (Figure 2b).[31] Photoluminescence (PL) spectrum of the sample also shows a red-shift of A-exciton peak due to the oxygen doping (Figure 2c; Figure S4d, Supporting Information). Proper oxygen doping in monolayer MoS_2 is beneficial to enhance its electrical properties by reducing the bandgap, increasing the carrier density, and improving intrinsic conductivity.[32–34]

To explore domain orientations in the MoS_2 films, we conducted second harmonic generation (SHG), transmission electron microscopy (TEM), and in-plane X-ray diffraction (XRD) measurements. The polarized SHG mapping is shown in Figure 2d. We can clearly see GBs and they are closed with no intersection, which is different from polycrystalline film. Note that the SHG mapping is a powerful tool to reveal the lattice

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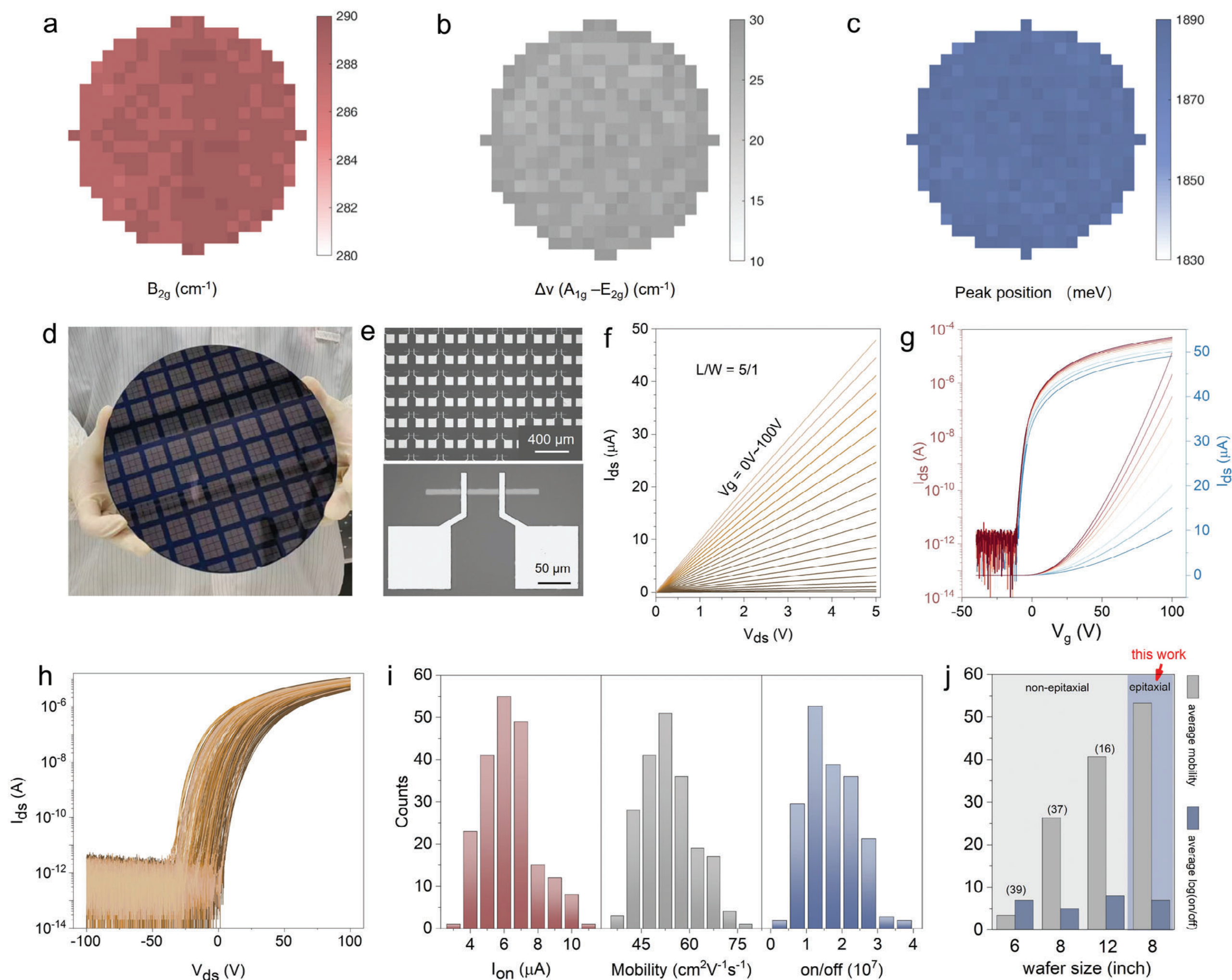

Figure 3. Uniformity characterizations of 8-in. monolayer MoS_2. a,b) Raman mapping of B_{2g} peak and $\Delta\nu$ ($A_{1g}-E_{2g}$) over the 8-in. wafer. c) PL mapping of the A-exciton peak over the 8-in. wafer. Both Raman and PL mappings were collected with a spatial resolution of 1 cm. d) Photograph of MoS_2 FETs fabricated on an 8-in. wafer. e) Optical images of the as-fabricated MoS2 FETs. f,g) Output and transfer curves of a typical MoS_2 FET. h) The transfer characteristics curves of 200 devices. i) Statistical distribution of I_{on}, mobility, and on/off ratio. j) Comparison of average mobility and on/off ratio of wafer-scale MoS_2.

symmetry of 2D materials and has been widely employed for the detection of the GBs.[35] Figure 2e shows the polar plots of two grains adjacent to a GB, and there is no detectable rotation between them. These two measurements reveal the anti-parallel orientation of domains. In addition, the polar plots are hexagonal symmetry, indicating the absence of uneven internal stress within the domains.[36] Next, a typical selected area electron diffraction (SAED) pattern is displayed in Figure 2f, exhibiting a single set of diffraction pattern with no distortion in the reciprocal space. Figure 2g shows a typical high-resolution transmission electron microscopy (HRTEM) image of monolayer MoS_2, illustrating two anti-parallel domains with a 4|4P GB. According to previous studies, this type of GBs is stable and negligible for the conductivity of monolayer MoS_2.[20,21]

Further, we performed in-plane XRD characterizations of the 8-in. monolayer MoS_2 wafer, with the incident X-ray beam nearly parallel to the sample surface. As illustrated in Figure 2h, $(10\bar{1}0)/(11\bar{2}0)$ diffraction peaks of MoS_2/sapphire could be seen and indicate the epitaxial nature of MoS_2 on sapphire with a 30° lattice rotation around the *c*-axis direction.[37] Importantly, the in-plane φ scan of both MoS_2 and sapphire wafers, as illustrated in Figure 2e, yielded six diffraction peaks with a 60° spacing, indicating that the 8-in. monolayer MoS_2 film was epitaxially grown on the entire 8-in. sapphire wafer.

4. Uniform and Wafer-Scale Devices

To assess the spatial uniformity of the as-grown 8-in. monolayer MoS_2, we performed Raman and PL mappings across the entire wafer with a 1-cm grid spacing (Figure S5, Supporting Information). The mapping data, including the B_{2g} peak, $\Delta\nu$ ($A_{1g}-E_{2g}$) and PL peak positions are shown in **Figure** 3a–c. These mappings suggest an excellent spatial uniformity of the monolayer MoS_2 at the 8-in. wafer scale. We transferred the as-grown monolayer MoS_2 films onto 8-in. SiO_2/Si wafers and fabricated 244 500 FETs across the entire wafer to evaluate the electrical uniformity

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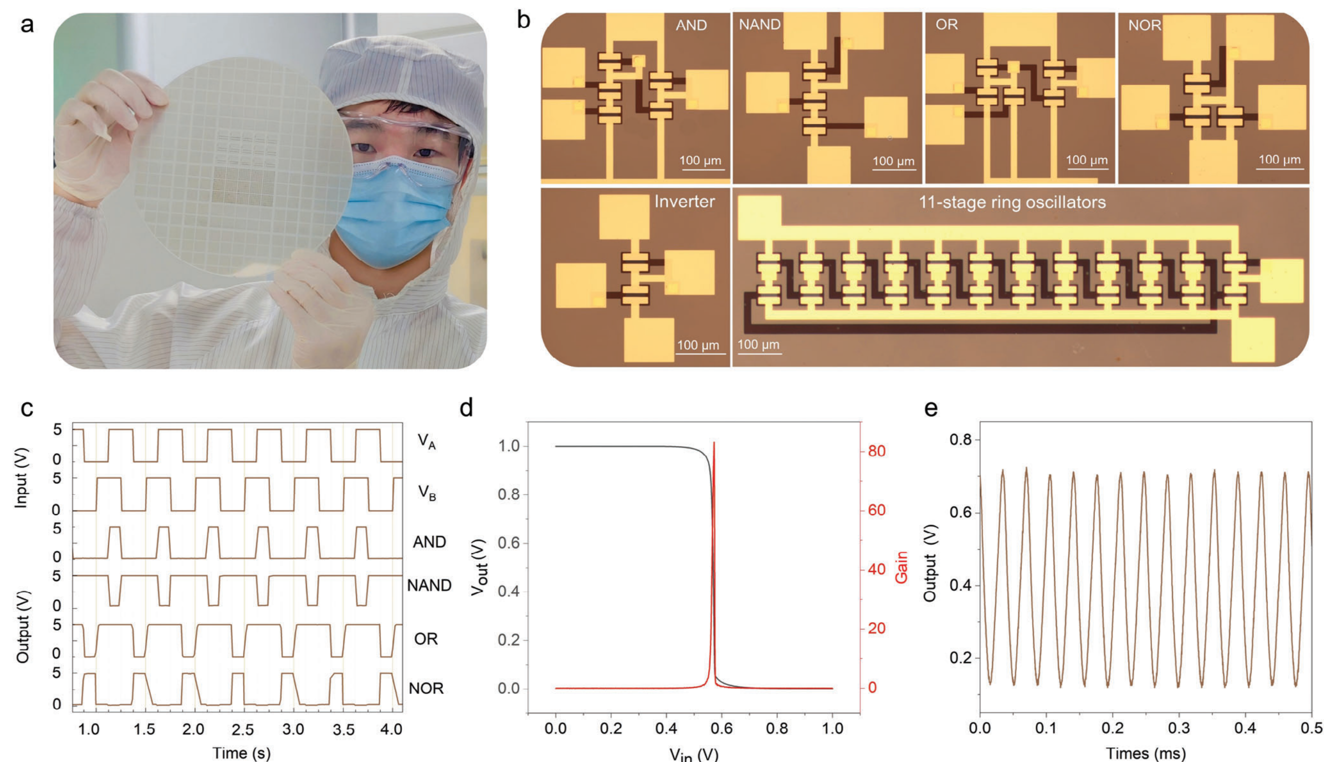

Figure 4. Logic circuits fabricated in batch based on 8-in. monolayer MoS_2. a) Photograph of 8-in. logic circuits on sapphire. b) Optical images of as-fabricated logic inverters, OR, NOR, AND, NAND gates, and 11-stage ROs. c–e) Output characteristics of AND, NAND, OR, and NOR gates (c), a logic inverter (d), and a 11-stage RO (e).

(Figure 3d). The detailed fabrication process and device structure are included in the Experimental Section and Figure 3e, respectively. The output and transfer characteristics curves of a typical MoS_2 FET with channel width (length) of 10 (50) µm are shown in Figure 3f,g, respectively. This device exhibits typical n-type transistor behavior with a high mobility of 73.2 $cm^2\ V^{-1}\cdot s^{-1}$ and on/off ratio of $>10^7$. Figure 3h shows the transfer characteristic curves of 200 randomly selected transistors, and the statistic analysis on the on-current (I_{on}), electron mobility, and on/off ratio are presented in Figure 3i. Notably, device-to-device variations are small with an average I_{on} of 6.8 µA, average mobility of 53.3 $cm^2\ V^{-1}\cdot s^{-1}$, and average on/off ratio of 2×10^7. It is worth noting that these benchmark performances are better than those previously achieved on wafer-scale polycrystalline monolayer MoS_2 (Figure 3i).[16,38,39]

Based on the as-grown 8-in. monolayer MoS_2 wafers, we also fabricated various logic circuits, including inverters, AND, NAND, OR, NOR gates, and 11-stage ring oscillators, as illustrated in **Figure** 4a,b. Note that these logic circuits were fabricated via a gate-first technology on sapphire, similar to that demonstrated in our previous work.[40] 30-nm thick Al_2O_3 dielectrics were employed in these devices with typical channel length/width of 10/40 µm. Typical characteristics of these logic circuits are shown in Figure 4c–e. All of them can function normally. These logic gates are operated with input signals of 5 V pulses (V_A and V_B) and exhibit accurate Boolean output functionalities. Figure 4d shows the output curves of a typical inverter with a high gain value of ≈80. In addition, we also assessed the performance of the 11-stage MoS_2 ring oscillators that integrated eleven cascading inverters along with an additional inverter employed as an output buffer for measurements. Figure 4e displays the output frequency, which reached 28 kHz for a typical 11-stage ring oscillator when powered by a supply voltage of 1 V.

5. Conclusion

We realize the epitaxial growth of 8-in. monolayer MoS_2 film on sapphire surface via the VCVD approach. The batch-fabricated MoS_2 FETs, AND, NAND, OR, NOR gates, inverters, and 11-stage ring oscillators also demonstrate exceptional electrical characteristics. We envision that such 8-in. wafer scale epitaxial monolayer MoS_2 would set a firm foundation for not only various large-scale applications such as integrated circuits but also for investigations of twistronics due to its high structural quality and large-scale uniformity. Although the present VCVD design is only compatible with only one wafer in each growth run, in principle, the multi-wafers growth can be realized by further enlarging the growth chamber and optimizing the growth conditions.

6. Experimental Section

CVD Growth of MoS_2: The substrate for MoS_2 epitaxy was 8-in. sapphire wafers (Wuhan Jingxin Optoelectronics Co., Ltd., c-face with a 0.2-degree miscut angle toward the *M*-axis). Prior to growth, substrates were annealed for 4 h at 1000 °C in an argon–oxygen mixture. The growth was

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performed in a home-made 10-in. three-zone VCVD system using pressed sulfur and MoO_3 powder as precursors. The sulfur (30–45 g) and MoO_3 (15–45 mg) precursors were placed in separate quartz containers flowed with carrier gases of Ar 100 sccm and Ar/O_2 40/2 sccm, respectively. For a monolayer MoS_2 growth, temperatures for each zone were set at 110–135 °C (for sulfur), 550–600 °C (for MoO_3), and 850–980 °C (for substrates), respectively. Note that the high growth temperature benefited to the low nucleation density and large domain size as a result. Besides, such high growth temperature also plays a key role on domain alignment on the sapphire (0001) surface during epitaxy. During the growth process, the pressure in the chamber was ≈2.32 torr. The growth of monolayer MoS_2 generally started from discrete nucleation on the sapphire substrate and growth of these nuclei, and finally, merged into a continuous film; the growth time was ≈50 mins.

Imaging and Spectroscopic Characterizations: The optical imaging was performed using a Nikon ECLIPSE Ni-U confocal microscope. Raman and PL spectra were collected by Horiba LabRam HR Evolution with an excitation laser wavelength of 532 nm. AFM imaging was carried out by the Asylum Research Cypher S. XPS measurements were performed on a Thermo Fisher ESCALAB XI+ instrument at a pressure of 10^{-10} mbar utilizing a monochromatic Al Kα X-ray source with an energy of 1486.6 eV. In-plane XRD measurements were obtained using a high-resolution diffractometer (Smartlab, Rigaku) with monochromatic Cu Kα1 radiation ($\lambda = 1.5406$ Å) at room temperature. SHG mapping was performed by the WITec alpha300R system with a laser excitation wavelength of 1064 nm and a power of ≈30 mW. SAED patterns were acquired using a Philips CM200 TEM operating at 200 kV; while, HRTEM characterizations were performed by a JEM ARM200F (JEOL, Tokyo, Japan) aberration-corrected scanning transmission electron microscope operating at 200 kV.

Device Fabrications and Measurements: 8-in. MoS_2 films were initially transferred from the sapphire substrates to 300-nm SiO_2/Si or another sapphire with back gate electrodes and stacks using the PMMA-assisted wet transfer method (refer to Data S6, Supporting Information). UV lithography (MA6, Karl Suss) and oxygen plasma etching (PlasmaPro 80 RIE, Oxford Instruments Company) were used for patterning. Source/drain contact electrodes were Au/Ti/Au (5/3/30 nm) deposited by e-beam evaporation. Gate electrodes and dielectrics were 2 nm-Ti/ 10 nm-Au/ 2 nm-Ti (deposited by e-beam evaporation) and 30 nm-HfO_2 (deposited by ALD), respectively. The electrical measurements were carried out in a four-probe vacuum (at 10^{-6} mbar) station equipped with a semiconductor parameter analyzer (Agilent B1500).

Simulations: The computational fluid dynamics (CFD) simulations were conducted using ANSYS Fluent software using the finite element analysis method. The simulation model was designed to match the dimensions of the actual vertical CVD system, with typical parameters set as follows: Ar flow rate of 380 sccm, chamber pressure of ≈2 Torr, and the density, thermal conductivity, and specific heat capacity characteristics of the quartz tube and sapphire substrate were assumed to be 2.65 g cm^{-3}, 0.91 W mK^{-1}, 892 J $kg^{-1}\cdot K^{-1}$, and 3.98 g cm^{-3}, 9.153 W mK^{-1}, and 1224.2 J $kg^{-1}\cdot K^{-1}$, respectively.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

H.Y., L.H., L.Z., Y.P., and X.L. contributed equally to this work. G.Z. supervised this project. H.Y., J.Z., S.W., and G.Z. designed and set the CVD system up. H.Y., L.H., and L.Z. performed the growth and microscopy, Raman and photoluminescence spectroscopy measurements. H.Y. performed XPS characterizations and fluid dynamics simulations. M.Z. helped in XRD characterizations. H.Y., S.W., H.D., and J.T. performed TEM characterizations. H.Y., P.Y., and K.L. performed SHG measurements. H.Y., L.H., Y.P., X.L., S.Z., and Y.Z. were responsible for sample transfer, device fabrication, and testing of the FET transistors. H.Y. and N.L. wrote the manuscript. All authors participated in the discussions and analysis of the results.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

2D semiconductor, chemical vapor deposition, epitaxial growth, monolayer MoS_2, wafer scale

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